A Comparative Study and Evaluation of Improved MAF- PLL Algorithms

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Received: 20.08.2016 Accepted:22.10.2016

Abstract-The Phase-Locked Loop (PLL) is a synchronization system widely utilized nowadays with the aim to achieve the correct operation of grid-tie PWM converters. The PLL based on Moving-Average-Filters (MAF-PLL) have recently received considerable attention thanks to their superiority over conventional methods in the case of severe grid disturbances. This paper provides an overview of recent improved MAF-PLL algorithms. A comparative study of the performance of four algorithms is also carried out through experimental tests performed for several types of grid faults. The results clearly show that the performance of each method is widely dependent on the grid fault type.

Keywords- PLL; MAF; grid faults; smart grid; Distributed Power Generation System (DPSGS).

1. Introduction

The correct and safe operation of the grid-tie Distributed Power Generation Systems (DPGS) requires a perfect and robust synchronization with the grid voltages. The latter are usually non-ideal because of the non-linear loads connected to the grid and various transient operations caused by the start-up of high power electrical machines and transformers. These disturbances make the perfect synchronization of any DPGS with the grid voltages a big challenge. This difficulty is mainly due to the waveform of the grid voltages at the point of Common Coupling (PCC) which is usually unbalanced and/or harmonically distorted. On the other hand, the synchronization of the DPGS with the grid voltages needs an accurate and fast estimation of the following two fundamental parameters: the instantaneous phase-angle and frequency of the voltage fundamental component at the PCC [1]. However, for most estimation algorithms, a tradeoff still exists between the two performances criteria i.e. the accuracy and rapidity.

A variety of synchronization techniques have been proposed in the scientific literature. Fig.1 hereafter gives the most popular algorithms which are classified into two main groups:

- Open-loop based synchronization methods: Their main advantages are the unconditional stability and satisfactory performances which are achieved only if the grid frequency is close to the nominal frequency.
- Closed-loop based synchronization techniques: They are in turn divided into two sub-groups:
  - Frequency-Locked Loops (FLLs)
  - Phase-Locked Loop (PLLs)

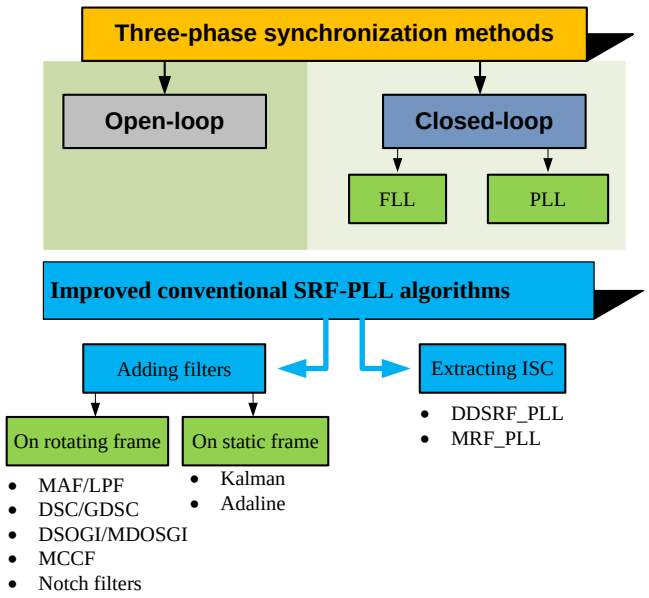

Figure 1. Classification of synchronization methods

Among the aforementioned algorithms, the PLLs remain until now the most popular because of to their easy real-time implementation and robust performance.

The basic PLL algorithm reports the grid voltages in a Synchronous Rotating Frame (SRF); it is therefore named the SRF-PLL. This algorithm enables a fast and accurate extraction of the grid parameters under ideal conditions [2]. Unfortunately, the performances of the SRF-PLL are highly degraded when the grid voltages are distorted or unbalanced. Indeed, unwanted frequency jitter appears in the estimated frequency and phase waveforms as reported in [3]. This weakness prevents the DPGS from remaining linked to the PCC under disturbed grid voltages. In order to overcome this limitation, a lot of improved PLL algorithms have been put forward in the last decade to make the SRF-PLL more robust against grid disturbances and therefore avoid the DPGS to be disconnected from the grid. We cite for example the SRF-PLL with an additional low-pass filter (LPF) [3], the PLL based on Adaptive-Notch-Filters [4], the Enhanced PLL [5], the Adaline neural networks [6], the Delayed Signal Cancellation [7, 8], and the PLL based on a dual generalized integrator of second order [9, 10]. Some other methods have used more than one filter like the PLL based on Multiple Complex Coefficient Filters [11], the PLL based on multiple generalized integrator of second order [12], and the PLL based on Generalized Delayed Signal Cancellation [13]. Another solution based on the use of more than one synchronous reference frame has also been developed with the aim to enable a better filtering of the harmonic components. We cite for example the PLL based on Multiple Reference Frames [14] and the PLL based on Double Decoupled Synchronous Reference Frames [15].

Although the aforementioned algorithms perform perfectly with unbalanced grid voltages, they lose their accuracy and provide a slow dynamic response for highly distorted voltages. Moreover, their implementation is more complex and they need additional computation time due to the use of multiple reference frames, multiple filters, delay operators, etc.

To overcome these serious limitations that appear when grid voltages are highly distorted, the low-pass filter usually included in the conventional PLLs is replaced by a Moving Average Filter (MAF). This filter has salient advantages including easy implementation, complete rejection of low-order harmonics and unbalanced voltages, low computational burden for real-time implementation, good immunity against noise, etc. A recent research work [16] has shown that the MAF-PLL is the most accurate synchronization algorithm for highly distorted grid voltages. However, this excellent behavior in a steady state results in a slow dynamic response. In order to tackle such a problem, various improved algorithms of robust MAF-PLLs have been proposed in the recent years.

This paper enriches the conference work [17] that provided a comprehensive review of most known MAF algorithms, which have been recently suggested to ameliorate the conventional MAF algorithm's dynamic response. The main novelty is the inclusion of experimental results which are utilized to compare and evaluate the improved MAF-PLL performances.

The manuscript is divided into four parts, including the introduction in section1. Section 2 presents an overview of the improved MAF-PLL algorithms. Section 3 provides a detailed comparative study and evaluation of these methods. Finally, a conclusion is given in section 4.

2. Overview of the Improved MAF-PLL Algorithms

This section describes the operation principle of a conventional MAF-PLL as the most popular improved algorithms. For each improved algorithm, we focus on the main differences referring to the conventional MAF-PLL.

2.1. Conventional MAF-PLL

Fig.2 depicts a simplified block diagram of the conventional MAF-PLL. As can be seen, the LPF usually utilized in the SFR-PLL scheme is now replaced by a moving average filter (MAF) with the aim of extracting the fundamental component of the grid voltages' positive sequence [18]. Therefore, two MAFs are applied after the abc/dq transformation (blue blocks in Fig.2).

In the continuous time domain the MAF transfer function is expressed as follows:

$$\bar{x}(t)=\frac{1}{T_w}\int_{t-T_w}^{t} x(\tau)\,d\tau \tag{1}$$

With $\bar{x}$ and x are the signals at the output and input sides of the filter. T_w the filter's window-width. Reporting equation (1) into the Laplace domain yields:

$$G_{MAF}(s)=\frac{1-e^{-sT_w}}{sT_w} \tag{2}$$

Where s stands for the Laplace operator. Substituting s with jw in equation (2) and making some mathematical

developments leads to the expressions of the filter's gain and phase such that:

$$G_{MAF}(jw) = \frac{2\left|sin(wT_w/2)\right|}{wT_w} \angle -\frac{wT_w}{2} \quad (3)$$

The Bode plot of the MAF's gain and phase versus the input signal's frequency is illustrated in Fig. 3. One can observe that for the frequencies near zero, the filter provides a unity gain. Moreover, for all frequencies $f = \frac{n}{T_w}, n \in N^*$, the MAF filter gain is quite equal to zero. This implies that the MAF filter preserves the entire input signal's DC component and completely removes all the components with the frequencies $f = \frac{n}{T_w}, n \in N^*$. This feature improves the PLL's steady state performance, making it more robust against the harmonic components content in grid voltages.

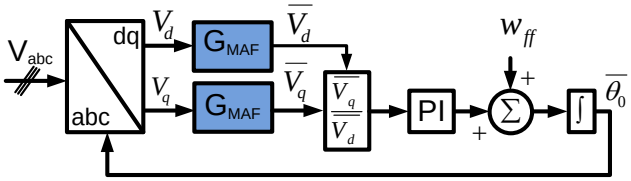

Figure 2. Conventional MAF-PLL block diagram

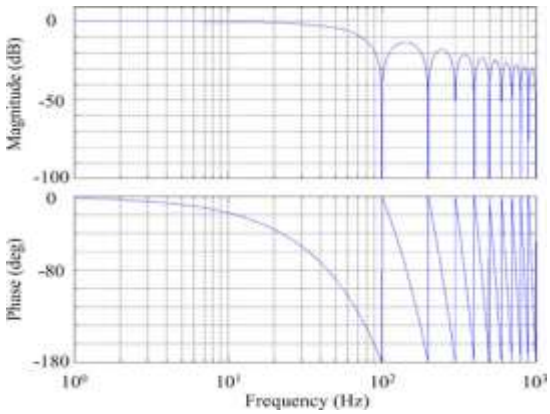

Figure 3. MAF bode plot for $T_w = 0.01s$

Theoretically, to achieve an ideal filtering, the window width T_w must be equal to $2/f_1$, where f_1 is the frequency of the input signal's fundamental component. Thus, the MAF can remove all the harmonics for a large value of T_w; that is to say, if some conditions are hold the filter acts as a perfect LPF [19]. Therefore, a better accuracy is achieved for a larger value of T_w. However, the increase of T_w decreases the system's bandwidth in open-loop. leading therefore to a slower dynamic response in closed-loop.

In practice, T_w is chosen so that $1/T_w$ is equal to the absolute value of the frequency of the lowest-order harmonic component content in the input signal. For disturbed grid voltages without DC components, the lowest-order harmonic component is due to negative-sequence fundamental component. Hence, by taking into account the dq transformation, this value is twice the grid nominal frequency. For the case of grid frequency equal for example to 50 Hz, the absolute value of frequency that corresponds to the negative sequence is equal to 100 Hz. Therefore, T_w = 1/100s. Unfortunately, this value is large enough so that it cannot ensure a fast dynamic behavior. This limitation has been the subject of a variety of research works that have been developed in recent years to improve the MAF-PLL's transient response. In the remaining of this section, we provide a comprehensive overview of the most known improved MAF based PLL algorithms.

2.2. *Improved MAF-PLL algorithms*

- DMAF-PLL [20] (Fig.4): It stands for a differential MAF-PLL. As a matter of fact, two extra proportional components (DFID and DFIQ), compared with a conventional MAF-PLL, are included with the aim of eliminating the lowest harmonic components before being applied at the input of the filter. This allows increasing the filter's bandwidth and consequently improves the dynamic closed-loop response.

- MAF-PLL with PLC [21] (Fig.5): In this case, a phase-lead-compensator (PLC) is added in the open-loop path. This PLC compensates the phase lag caused by the MAF and therefore improves the dynamic response [6].

- QT1-PLL (Fig.6): It stands for a quasi-type-1 PLL. In this case, the controller consists of a simple proportional gain K_p instead of the conventional PI regulator used in the MAF-PLL. Note that, the elimination of the integral term worsens the tracking performances of the frequency drifts. To overcome this limitation, the same signal applied at the input block of the proportional gain is also added to the value of the estimated phase angle [22]

The three aforementioned improved MAF-PLLs are considered as the most popular algorithms. Note that many other synchronization schemes based on MAF have been proposed in the literature. We cite for example:

- HPLL (Fig.7): It stands for a Hybrid-PLL [23]. As compared with the QT1-PLL, this algorithm uses two additional delayed cancellation blocks that are inserted between the two coordinate transformation blocks, (abc, αβ) and (αβ, dq). Theoretically, this algorithm provides better performances than he QT1-PLL only if even-order harmonics are present in the grid voltages.
- The PLL with MAF- based prefiltering stage (PMAF-PLL) depicted in Fig.8 [24]. This method removes the MAF block from the open-loop path of the PLL. This block is replaced by a MAF based prefiltering stage placed at the input of the PLL.
- The MAF (PID) [19]: a derivative term is added in the expression of the PI controller to accelerate the dynamic response.
- The Modified Demodulation Technique (MDT) [25]: (Fig.9 and Fig.10) A modified demodulation method was utilized to remove the lowest-order harmonic component as shown in Fig.9. The operating principle of the demodulation block diagram is explained in Fig.10.

- The WLSE_PLL_Algorithm [26, 27]: the WLSE and Zero Crossing Detection (ZCD) techniques are implemented together with the FLL to improve the dynamic response and achieve an accurate frequency adaptation as shown in Fig.11. All the aforementioned improved MAFs are classified in Fig.12.

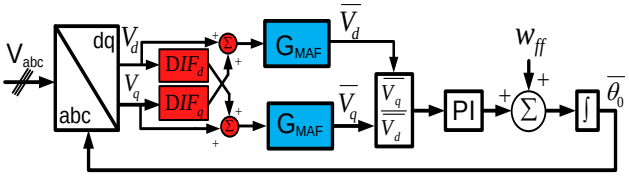

Figure 4. DMAF-PLL block diagram

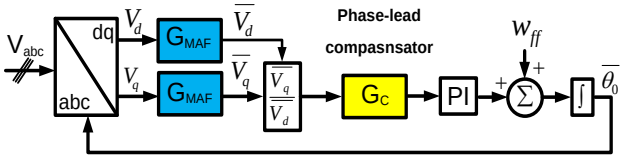

Figure 5. MAF-PLL with PLC block diagram

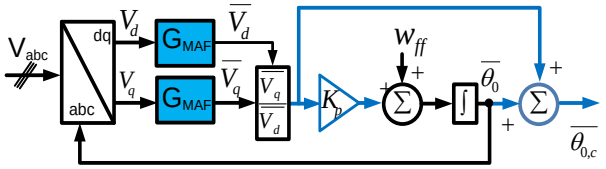

Figure 6. QT1-PLL block diagram

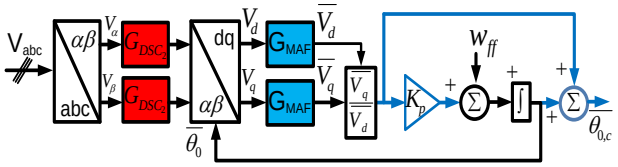

Figure 7. HPLL block diagram

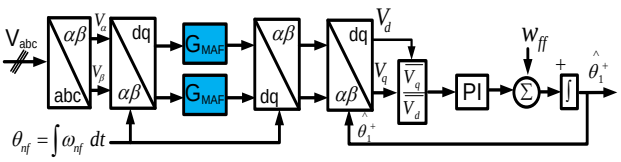

Figure 8. PMAF block diagram

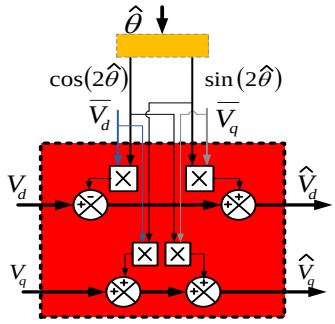

Figure 9. DFC unit block diagram

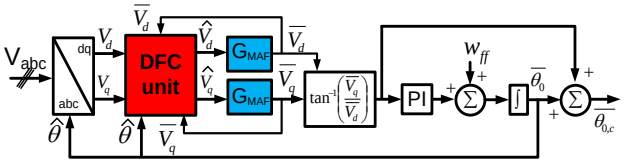

Figure 10. MDT block diagram

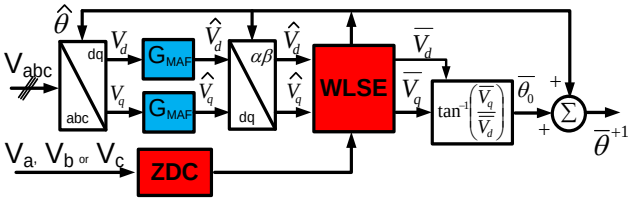

Figure 11. WLSE_PLL block diagram

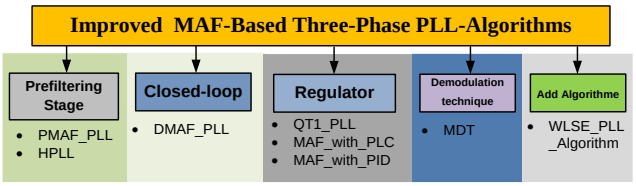

Figure 12: Classification of improved MAF_PLL

3. Experimental Tests and Comparative Study between the Improved MAF-PLL Algorithms

The main aim of this section is to make a comparative study of the following improved MAF PLL algorithms: DMAF-PLL, MAF with PLC, QT1-PLL. This comparative study is based on experimental results where all algorithms are implemented in real-time on the DSP TMS320F28335 of Texas Instruments. For all tests, the fundamental frequency of the grid voltages is set to 50 Hz. Accordingly, the window-width of the MAF is fixed to 0.01 s which is equal to $1/(2*50)$. The evaluation of the algorithms' performances is based on two fundamental criteria:

- The frequency error's dynamic response.
- The phase error's dynamic response.

These performances are evaluated with four cases of grid voltages disturbances:

Case 1: 3 Hz grid frequency jump
Case 2: -20°Grid phase jump

Case 3: voltage sag: 50% abrupt decrease of the three-phase voltages amplitudes with -20° phase jump.
Case 4: distorted grid voltages including the harmonic components listed in table 1.

Table 1. Harmonic components content in the grid voltages for the test of case 4

Sequence / *Order*	*Content*
-1	10%
-5	9%
+7	8%
-11	7%
+13	5%

3.1. Case 1: 3 Hz grid frequency jump

Fig.13 and Fig.14 illustrate the frequency and phase errors. We can conclude the following remarks:
- Frequency error: All the improved algorithms provide a better dynamic response as compared to the conventional MAF-PLL. The best settling times are achieved with the DMAF-PLL and QT1-PLL algorithms.
- Phase error: It is clear that the DMAF-PLL algorithm provides the best transient response.

Consequently, the best performance following a frequency jump is obtained with DMAF-PLL.

3.2. Case 2: – 20° grid phase jump

The obtained results are illustrated in Fig.15 and Fig.16. The following remarks can be concluded:
- Frequency error: All the improved MAF-PLLs algorithms provide a faster dynamic response than the conventional MAF-PLL as expected. The best dynamic response is achieved with DMAF-PLL and QT1-PLL. However, it can be observed that the DMAF-PLL provides a larger overshoot than the QT1-PLL.
- Phase error: All the improved algorithms perform a faster transient response than the conventional MAF-PLLs. On the other hand, the three-algorithms (QT1, DMAF, MAF-PLC) provide approximately the same settling time during the transient response.

It can therefore be concluded that the QT1-PLL gives the best performances in case of phase jump type of grid disturbance.

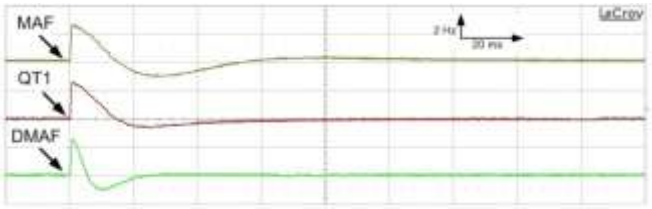

Figure 13. 3-Hz-grid-frequency-jump frequency error responses.

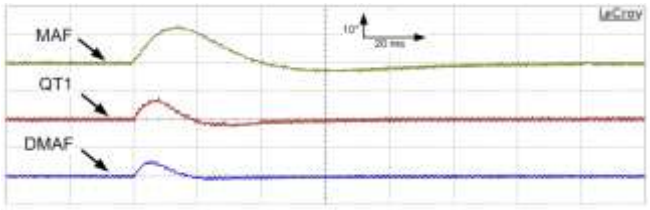

Figure 14. Phase error responses with a +3 Hz grid frequency jump.

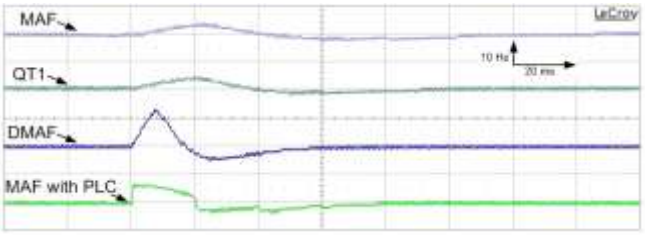

Figure 15. -20°grid-phase-jump frequency error responses.

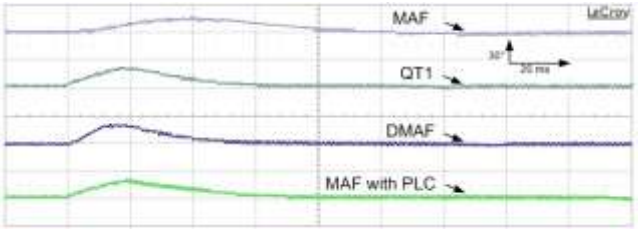

Figure 16. -20° grid-phase-jump phase error responses.

3.3. Case 3: voltage sag: 50% abrupt decrease of the three voltages amplitudes with -20° phase jump

Fig.17 displays the waveforms of the grid voltages before and after the described disturbance. The frequency and phase errors responses are displayed in Fig.18 and Fig.19 respectively.
- Frequency error: the fastest transient response is provided by the DMAF-PLL and QT1-PLL algorithms. One can also observe a remarkable overshoot occurring with the MAF-PLC algorithm.
- Phase error: the best dynamic behavior is achieved with QT1-PLL and MAF_PLC respectively. Note that, the settling time obtained with the MAF-PLC PLL is slightly lower than the one achieved with the QT1-PLL.

As a consequence, one can deduce that the QT1-PLL algorithm provides the best performances in case of this type of voltage sag.

3.4. Case 4: Harmonically distorted grid voltages including the low-order components listed in table 1

Figure 20 illustrates the distorted grid voltages waveforms utilized for this test. The phase error responses are shown in Fig.21. As expected, all improved algorithms provide a faster dynamic response as compared to the conventional MAF-PLL. However, their transient overshoots are larger than the one of the MAF-PLL. It can also be observed, that the DMAF-PLL provides unwanted

oscillations in steady state operation which is an important limitation of this algorithm.

Among the four responses, it is clear that the QT1-PLL is the best algorithm for this type of grid disturbances including low-order harmonics and without any variation of the fundamental frequency.

Table 3 hereafter summarizes the performances regarding the four cases of grid disturbances of the improved MAF-PLLs tested in this paper. We added also the performances of the HPLL which are almost the same as those of the QT1-PLL.

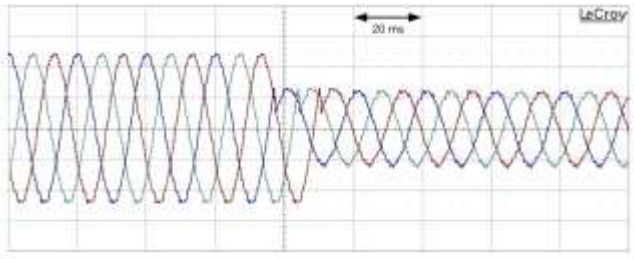

Figure 17. Voltages sag with a 50% decrease of the amplitude and -20° phase jump

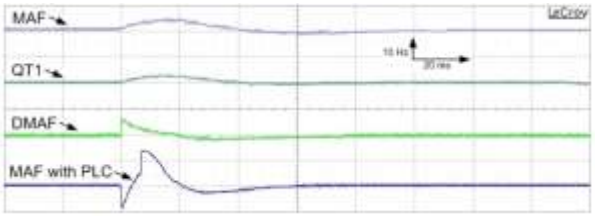

Figure 18. Frequency error responses with voltage sag

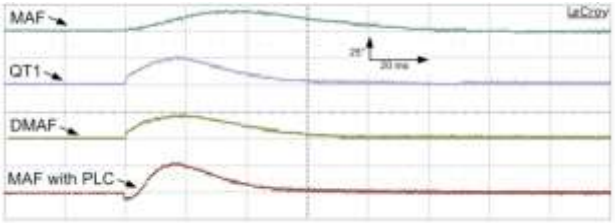

Figure 19. Phase error responses with voltage sag

3.5. Average computational time for each improved MAF_PLL

The computational time is a performance criterion of an amount importance. Indeed, the best algorithm is the one that refers to a low cost implementation. The aforementioned algorithms are executed in real-time on the DSP TMS320F28335 operating at 150 MHz. Upon the obtained results, shown in Table 2, we can observe that the conventional MAF-PLL and the DMAF-PLL need less computational time. The MAF_ PLC is the worst algorithm basing on this performance criterion.

4. Conclusion

A comparative study is performed in this paper between four improved MAF-PLL algorithms which have been put forward in the recent works in order to enhance the conventional MAF-PLL's dynamic response. Many experimental tests are carried out for four types of grid faults. The following conclusions can be retained:

- All the improved MAF algorithms provide a faster dynamic behavior than the conventional one i.e. MAF-PLL.
- The QT1-PLL provides the best performances in cases of grid phase jump, voltage sags, and distorted grid voltages without variation of the fundamental frequency.
- The DMAF-PLL gives the best performances in case of fundamental frequency variation. However, it suffers from unwanted steady-state oscillations in case of distorted grid voltages. It provides also a large frequency overshoot in case of phase jump type of grid fault.

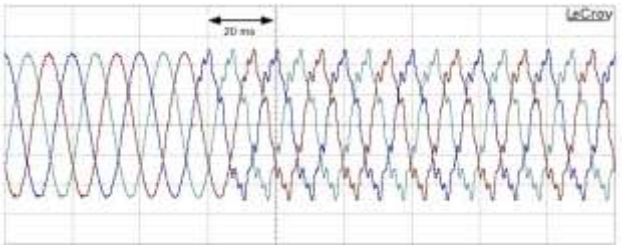

Figure 20. Grid voltages waveforms including the low harmonic components listed in table 1

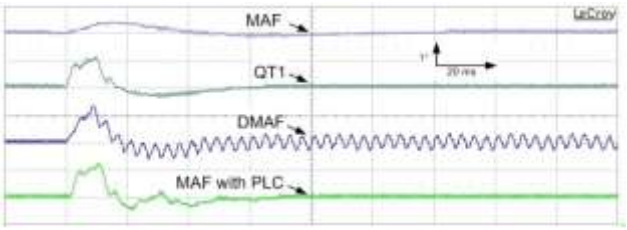

Figure 21. Phase error responses in case 4

Table 2. Average execution time

PLL	Average execution time(µs)
MAF-PLL	23.265
DMAF-PLL	23.818
QT1-PLL	26.799
MAF_ PLC	45.590

Table 3. Summarized performances of the improved MAF-PLL

Cases / Improved MAF-PLLs	1		2		3		4
	Frequency error	Phase error	Frequency error	Phase error	Frequency error	Phase error	Phase error
DMAF-PLL	+	+	-	+	+	0	-
QT1-PLL	+	0	+	+	+	+	+
HPLL	+	0	+	+	+	+	+
MAF_ PLC	0	0	0	+	-	0	0

"+" "0" and "-" means respectively good, fair and weak performances

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