A Novel High-Gain Cuk-Sepic Converter with Coupled Inductor for Renewable Energy Applications

Shujie Mu [*], Fuyu Ling [*‡], Na Li [*], Jiaqi Wang [*] Ilhan Garip [**]

[*]Department of Electrical Engineering, Yingkou Institute of Technology, Liaoning Yingkou

[**] Faculty of Engineering and Architecture, Beykoz University, Istanbul, Turkey

(Esmaeilzadeh786@hotmail.com, fuyu2125@gmail.com, Na23462@gmail.com , Jiaqi2024@hotmail.com, ilhangarip60@gmail.com)

[‡] Corresponding Author; Fuyu LING, Department of Electrical Engineering, Yingkou Institute of Technology, Liaoning Yingkou

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Abstract- The increase in photovoltaics, fuel cells, and power cells as a proportion of our energy structure can reduce dependence on traditional energy sources, which can result in energy conservation, emission reduction, and sustainable development. Power grid development has increasingly focused on integrating distributed energy and power grids. It proposes a technology for integrating the Sepic-converter and Cuk-converter. A primary winding is created from the Sepic's intermediate energy storage inductor. A capacitor is added to the secondary winding to generate a voltage-doubling structure. Performance and efficiency are improved with this method. It maintains the continuous input and output current characteristics of the Cuk converter, making it compatible with DC buses and photovoltaic arrays. It is the passive clamping capacitor that absorbs the leakage inductor energy. The parasitic capacitance and switch are thereby reduced, and the switch is also subject to low voltage stress. This paper explores the working principle, performance parameters, and operating conditions of the converter in detail. Finally, an experimental platform was used to produce a 150W prototype. Experimental results were used to test and verify the validity of the previous theoretical analysis.

Keywords: Coupled inductor, high gain, passive clamp, voltage stress.

1. Introduction

With the advent of the new century, due to the continuous consumption of fossil energy, countries around the world pay more and more attention to clean energy. New energy represented by the photovoltaic, fuel cell and power cell has been vigorously developed. To achieve sustainable development through energy conservation, it must increase the proportion of clean energy in our energy structure and decrease our dependence on traditional energy sources. Distributed power generation has the characteristics of energy utilization nearby, low price, and flexible installation. The grid connection of distributed power generation has become the main direction of power grid development at present [1-5]. Clean energy sources, such as fuel cells, typically produce a DC output voltage that is often too low to meet the voltage requirements for grid connection. Therefore, it is necessary to boost its output voltage and supply it to DC loads such as grid-connected inverters. In recent years, there has been a significant amount of research conducted by universities and scholars worldwide on high-voltage gain DC converters, resulting in numerous achievements [6-10]. It introduces the switched inductor structure into the Sepic converter and realizes the gain improvement of the converter through the parallel series discharge of two inductors [11]. In their proposal, [12] suggests an active switch inductor structure that builds upon the switched inductor design. This is achieved by replacing the diode in the switched inductor with a switch tube, which in turn decreases voltage stress on the switch tube while also improving voltage gain. It improves the output capacitor voltage doubling structure based on an active switching inductor and further increases the voltage gain [13]. It expands and summarizes the converter with a switched-capacitor structure [14]. However, the voltage regulation range of the converter using a switching capacitor is small, and when it is applied to the input terminal, it will produce a large current impact. Generally, the coupling inductance is added to a converter to suppress the current impact and enhance voltage gain [15-16]. The voltage gain of conventional converters can be increased by applying topology combination technology. This method involves overlaying two distinct converter topologies to enhance voltage gain without sacrificing the original characteristics of the converter. It developed a high-gain Boost-Sep converter by combining the Boost and Sepic converter [17]. Similarly,

[18] suggests a high-gain Buck-Boost-Zeta converter achieved through the combination of two Buck-Boost-Zeta converters. Other combined converters are proposed in reference [19-21], and will not be described here. Based on this study a combined Cuk-Sepic converter. Simultaneously, the converter incorporates a voltage-doubling structure through a coupling inductance, which enhances its voltage gain. Additionally, a clamp branch is employed to decrease the voltage spike of the switch. Both the input and output terminals of it possess inductance, resulting in minimal current ripple [22-23].

2. Analysis of the Proposed Converter

2.1. Proposed Converter

The Cuk converter and Sepic converter are two DC-DC converters with step-down functions and have the same input energy storage structure, so the two converters can be integrated to get the integrated Cuk-Sepic converter. Then the voltage doubling structure of the coupling inductor is introduced into the integrated Cuk-Sepic converter, and a high-gain integrated Cuk-Sepic converter with a Euro-Russian inductor is obtained. The topology formation process of the converter mentioned above is shown in Figure 1. Before analyzing the operating principle, the coupling inductance structure is replaced with an equivalent one. This new structure consists of an ideal transformer with L_k in series and an excitation inductance L_m in parallel, with a turn ratio of n. The homonymous end is denoted by the symbol "*". Figure 2 exhibits the equivalent topology.

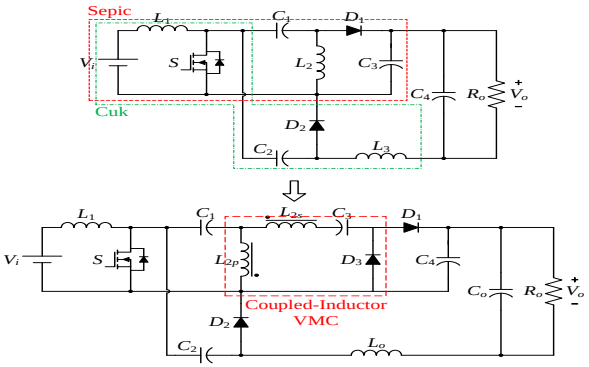


Fig.1. The proposed converter topology.

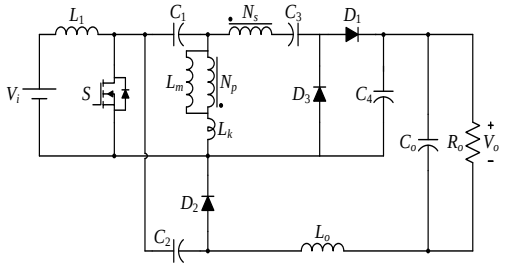


Fig. 2. Equivalent topology of the designed converter.

2.2. Working principle of the proposed converter

Assuming that the input inductance Li, excitation inductance Lm, and output inductance Lo are very large, the converter is operated in continuous conduction mode (CCM). The operating waveforms and working modes are shown in Fig. 3 and Fig. 4 (a)~(e).

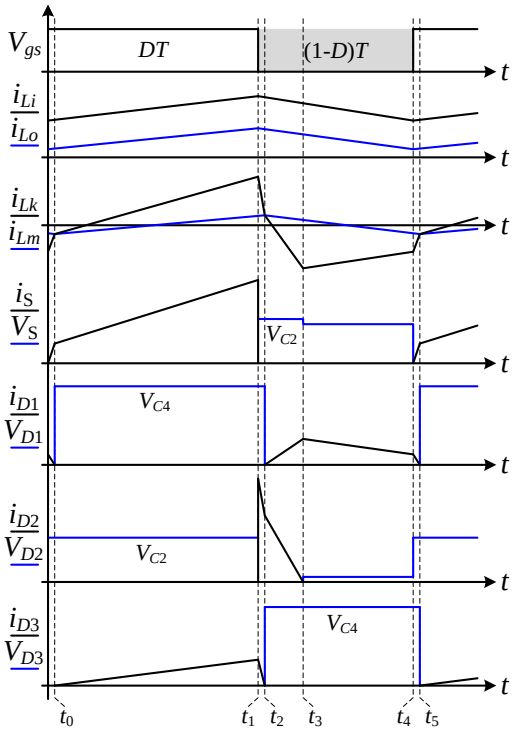
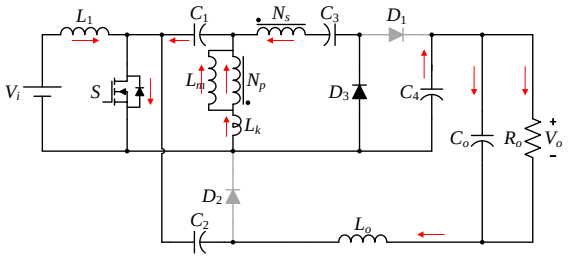
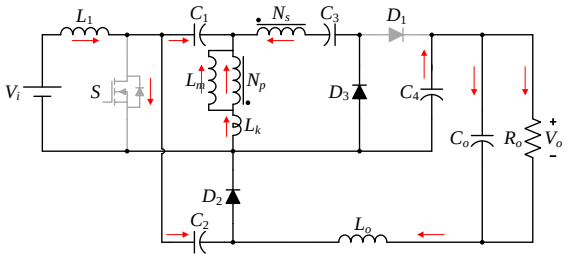


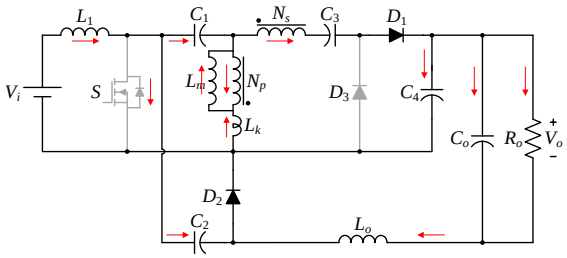
Fig. 3. Operating mode waveforms.



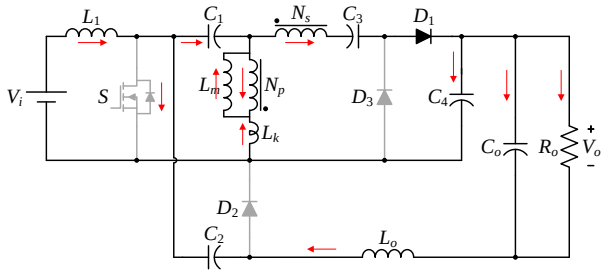
(a) Operating mode 1[t0~t1]



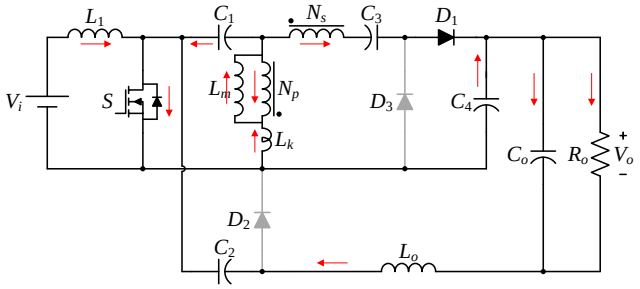
(b) Operating mode 2[t1~t2]



(c) Operating mode 3[t2~t3]



(d) Operating mode 4[t3~t4]



(e) Operating mode 5[t4~t5]

Fig. 4. Working mode of the converter.

Operating mode 1 [~]: as shown in Figure 4 (a), switch tube S has been opened in the previous mode, the diode is on, and are closed in reverse; The input inductor is provided with energy storage by the power supply, the primary side of inductor is provided with energy storage by the capacitor, and the current, and increase linearly; The secondary side series capacitor offers energy to the capacitor through S and; The capacitor and are linked in series through S to offer energy storage for the output inductor, the current increases linearly. The expressions of current and are [2]:

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_0) + \dfrac{V_{C3} - V_{C1}}{nL_m}(t - t_0) \\ i_{Lk}(t) = i_{Lk}(t_0) + \dfrac{(n+1)V_{C1} - V_{C3}}{nL_k}(t - t_0) \end{cases} \quad (1)$$

Working mode 2 [~]: as Figure 4 (b), at , the switch tube S is off, diodes D1, and D2 are on, and D1 is closed in reverse. The capacitance absorbs the energy via the diode, the current reduces rapidly, and the current also starts to decrease, which is a short process. At, the current drops to zero. The expressions of current and are [3]:

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_1) + \dfrac{V_{C3} + V_{C2} - V_{C1}}{nL_m}(t - t_1) \\ i_{Lk}(t) = i_{Lk}(t_1) + \dfrac{(n+1)(V_{C1} - V_{C2}) - V_{C3}}{nL_k}(t - t_0) \end{cases} \quad (2)$$

Working mode 3 [~]: As Figure 4 (c), the switch tube S is still off, and the and are on, is turned off in reverse. The capacitance continues to absorb the energy and the current continues to decline; The input inductor charges the capacitor, and reduces linearly; The secondary side is linked in series to enhance via the; The offers power to the load via, and the reduces linearly; At, decreases to zero, the mode ends. The expressions of current and are [4]:

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_2) + \dfrac{V_{C2} + V_{C3} - V_{C1} - V_{C4}}{nL_m}(t - t_2) \\ i_{Lk}(t) = i_{Lk}(t_2) + \dfrac{(n+1)(V_{C1} - V_{C2}) - V_{C3} + V_{C4}}{nL_k}(t - t_2) \end{cases} \quad (3)$$

Working mode 4 [~]: as shown in Figure 4 (d), the switch tube S remains off, the diode is on, and is cut off; Capacitance C1 is continuously charging by the input inductor L1. , The load energy is continuously provided by Lo, and the current and current continue to enhance linearly; The capacitor C4 is continuously charged by Ns. The expressions of current and are [5]:

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_3) + \dfrac{V_{Lk} + (n+1)V_{Lm} + V_{C4} - V_{C3}}{nL_m}(t - t_3) \\ i_{Lk}(t) = \dfrac{i_{Lm}(t) - n\left[i_{Li}(t) + i_{Lo}(t)\right]}{n+1} \end{cases} \quad (4)$$

Working mode 5 [~]: as shown in Figure 4 (e), the switch S, and diode D1 are on, and the diodes D2 and D3 are cut off. The power supply Vin starts charging the input inductor and starts to increase; Capacitance stores energy for the coupling inductor, the current starts to rise rapidly, the current decreases rapidly, and at the moment, the diode D3 is turned off as the current iNs is decreased to zero. The expressions of current and are [7]:

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_4) + \dfrac{V_{C3} - V_{C1} - V_{C4}}{nL_m}(t - t_4) \\ i_{Lk}(t) = i_{Lk}(t_4) + \dfrac{(n+1)V_{C1} - V_{C3} + V_{C4}}{nL_k}(t - t_4) \end{cases} \quad (5)$$

3. Steady-State Performance Analysis

3.1. Voltage Gain Analysis

The coupling coefficient k can be expressed as [8]:

$$k = \frac{L_m}{L_m + L_k} \quad (6)$$

When performing steady-state performance, only mode 1 and mode 3[17] can be considered in the analysis because mode 2 and mode 5 are transition modes with short duration. When it works in operating mode 1, from Figure 4 (a), there are [9]:

$$\begin{cases} V_{Li} = V_{in} \\ V_{Lm} = kV_{in} \\ nV_{Lm} = V_{C3} - V_{C1} \\ V_{Lo} = V_{C2} + V_{C4} - V_o \end{cases} \quad (7)$$

Under the condition of switch S is turned off, the converter is operating in operating mode 3, according to Figure 3 (c), there are [10]:

$$\begin{cases} V_{Li} = V_{in} - V_{C2} \\ V_{Lm} = k(V_{C1} - V_{C2}) \\ nV_{Lm} = V_{C2} + V_{C3} - V_{C1} - V_{C4} \\ V_{Lo} = V_{C4} - V_o \end{cases} \quad (8)$$

Based on the voltage-second balance criteria of the input inductor, combining Formulas (7) and (8), the capacitor voltage can be expressed as:

$$V_{C2} = \frac{1}{1-D} V_{in} \quad (9)$$

Based on that criterion of excitation inductance, combining Formulas (7), (8) and (9),

$$V_{C1} = V_{in} \quad (10)$$

Take Formula (9) and Formula (10) back to Formula (7) and Formula (8), and the voltage expressions of Capacitance and Capacitance are respectively:

$$V_{C3} = (1+nk)V_{in} \quad (11)$$

$$V_{C4} = \frac{1+nk}{1-D} V_{in} \quad (12)$$

Based on that criterion of, combined with formulas (9) and (12), the voltage gain G of converter is obtained:

$$G = \frac{V_o}{V_{in}} = \frac{1+D+nk}{1-D} \quad (13)$$

Based on formula (13), The 3D surface graphs of the voltage gain for different turn ratios are given in Figure 5. The voltage gain G is increased by adding the turns ratio n, but it decreases as the coupling coefficient k decreases. Therefore, in practice, the two windings of a coupled inductor are coupled as completely as possible and the appropriate turn ratio should be selected according to the application situation.

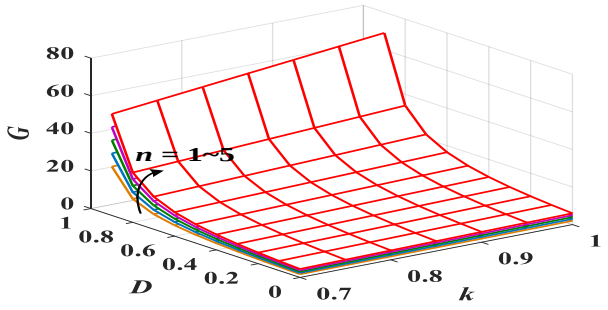


Fig. 5. The association between voltage gain G and k and duty cycle D.

When k=1, base on formula (13), the voltage gain can be calculated as:

$$V_{vs-S} = \frac{1}{1-D} V_{in} = \frac{1}{1+D+n} V_o \quad (14)$$

3.2. Device Voltage and Current Stress

3.2.1. Voltage stress

The voltage stress of semiconductor devices was obtained as follows:

$$V_{vs-S} = \frac{1}{1-D} V_{in} = \frac{1}{1+D+n} V_o \quad (15)$$

$$V_{vs-D1} = V_{vs-D3} = \frac{1+n}{1-D} V_{in} = \frac{1+n}{1+D+n} V_o \quad (16)$$

$$V_{vs-D2} = \frac{1}{1-D} V_{in} = \frac{1}{1+D+n} V_o \quad (17)$$

3.2.1. Device current stress

Based on the second balance criteria, the mean current of D1~D3 is equal to the output current, which can be calculated as:

$$I_{Li} = \frac{(1+D+n)^2}{R(1-D)^2} V_{in} \quad (18)$$

$$I_{Lo} = \frac{1+D+n}{R(1-D)} V_{in} \quad (19)$$

$$I_{Lm} = 0 \quad (20)$$

The max current stress of the switch can be calculated as:

$$I_{S(peak)} = I_{Li} + I_{Lo} + \frac{\Delta i_{Li} + \Delta i_{Lm} + \Delta i_{Lo}}{2} + \frac{(1+n)I_o}{D} \quad (21)$$

The expressions of current stress of the secondary tube, and are as follows:

$$I_{D1(peak)} = \frac{I_o}{1-D} \quad (22)$$

$$I_{D2(peak)} = I_{Li} + I_{Lo} + \frac{\Delta i_{Li} + \Delta i_{Lm} + \Delta i_{Lo}}{2} + \frac{(1+n)I_o}{D} \quad (23)$$

$$I_{D3(peak)} = \frac{I_o}{D} \quad (24)$$

3.3. L_i, L_o and Excitation Inductance L_m Critical Conditions

Since the converter is a combination of the Sepic and the Cuk converter, there is a certain relationship between the inductance and the intermittent condition of inductance, and excitation inductance. The main waveform of it under DCM mode (Continuous Conduction Mode) is shown in Figure 6.

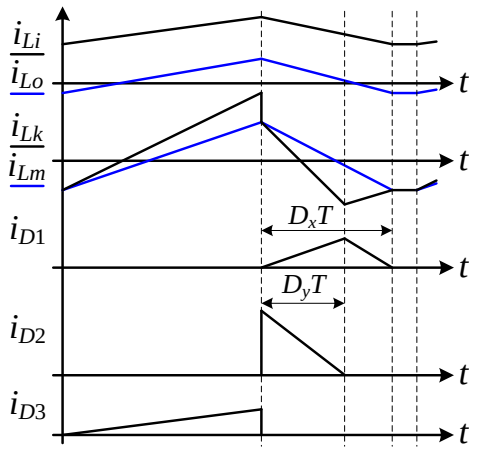


Fig. 6. Simplified waveform of converter DCM.

Assume that the current of the sum of current, and excitation inductance current and its peak value is:

$$i_{Leq} = \frac{V_{in}DT}{L_o} + \frac{V_{in}DT}{L_i} + \frac{V_{in}DT}{L_m} = \frac{V_{in}DT}{L_{eq}} \tag{25}$$

Where is equivalent inductance, and its expression is:

$$L_{eq} = \frac{L_o L_i L_m}{L_i L_m + L_o L_m + L_i L_o} \tag{26}$$

Based on the diodes D1 and D2, the following voltage equation can be express as:

$$I_{D1} = I_o T = \frac{1}{2} \cdot \frac{1}{1+n} \cdot \frac{D_x - D_y}{D_x} i_{Leqp} D_x T \tag{27}$$

$$I_{D2} = I_o T = \frac{1}{2} i_{Leqp} D_y T \tag{28}$$

The expression of duty cycle obtained from Equations (27) and (28) is:

$$D_x = \frac{2(2+n)I_o}{i_{Leqp}} \tag{29}$$

Time constant of assumed equivalent inductance τLeq is:

$$\tau_{Leq} = \frac{L_{eq}}{RT} \tag{30}$$

Under condition of duty cycle is, the converter operates in BCM mode (Boundary Conduction Mode), combining formulas (29) and (30), the equivalent inductance critical time constant is obtained as follows:

$$\tau_{LeqB} = \frac{D(1-D)^2}{2(2+n)(1+D+n)} \tag{31}$$

The critical time constant curve is drawn according to Equation (31) as shown in Figure 7. When, it works in CCM mode, and vice versa, it works under DCM mode.

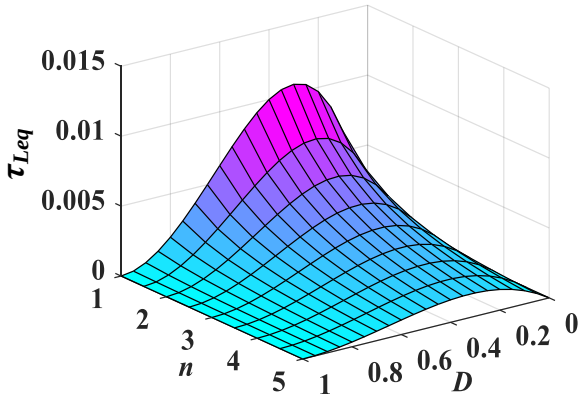


Fig. 7. Critical time constant surface.

3.4. Comparison of Converter Performance

In this paper, it proposes a converter and compare it to another converter with coupling inductance that has been proposed in other documents. The comparison can be found in Table 1.

Table 1. Parameters comparison of converter

Converter	Voltage Gain (Vo/Vin)	Switch Tube Stress (Vvs/Vo)	Input and Output Current Continuity
Boost	$\frac{1}{1-D}$	1	Input Continuous
Reference [17]	$\frac{1+D(n+1)}{1-D}$	$\frac{1}{1+D(n+1)}$	Output Continuous
Reference [18]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	Input Continuous
This Paper	$\frac{1+D+n}{1-D}$	$\frac{1}{1+D+n}$	Input and Output are Both Continuous

The converter proposed in this paper has the following advantages: higher voltage gain, lower voltage stress, and continuous input and output currents. Compared to other converters proposed in the literature. These characteristics suggest that the converter proposed in this paper is a better choice for many applications.

4. Simulation and Experiment

4.1. Converter Parameter Setting

To ensure the accuracy of the theoretical analysis, it is essential to construct a simulation system for the converter and establish its parameters. This can be achieved by determining the parameters of the converter through the following steps:

1) Input voltage 24V, output voltage 200V, power 150W;

2) Inductance, Excitation inductance, leakage inductance, turn ratio;

3) Capacitance

4.2. Matlab/PSIM Joint Simulation System

Because PSIM is a software specially used for power electronic system simulation, its simulation speed is fast, and its convergence is high, and it is suitable for building the main circuit of coupled inductor Cuk-Sepic converter, in contrast Matlab is widely used in the design of control system. Therefore, in this paper, through the Simcoupler interface program in PSIM, the main circuit built in PSIM is imported into Matlab to realize Matlab/PSIM joint simulation. The joint simulation diagram is shown in Figure 8.

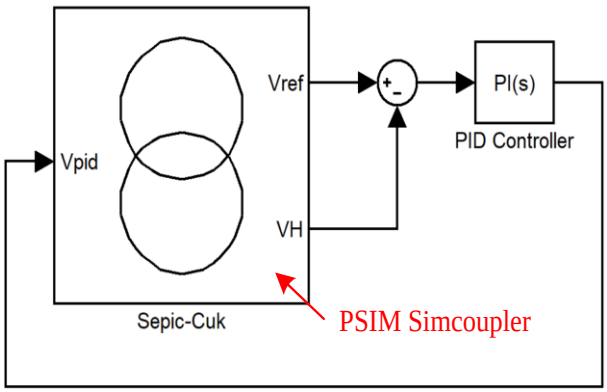


Fig. 8. Schematic diagram of joint simulation.

The frequency sweep method is commonly used in engineering to scan the transfer function of a converter, which helps in designing its control system. By building a model in Matlab and using the Linear Using the Analysis toolbox, the minor signal frequency is swept and fitted to draw the transfer function as shown in Figure 9. As can be seen, the traversing frequency of the Bode diagram is about 14.5k, the phase margin is about 13, and the system is unstable.

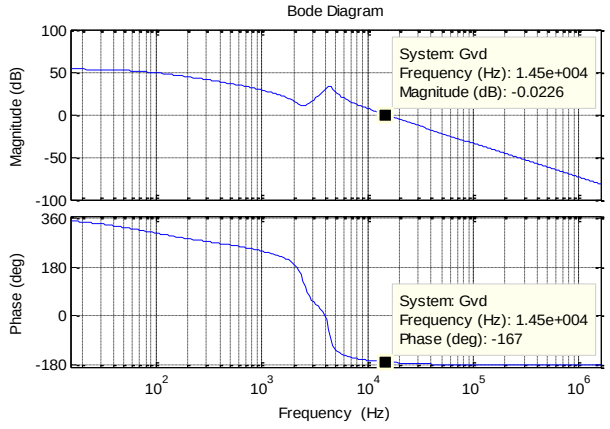
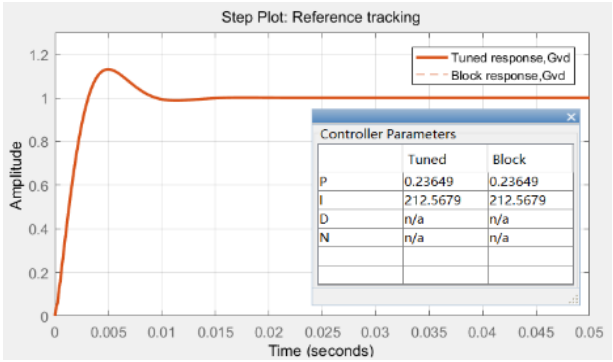
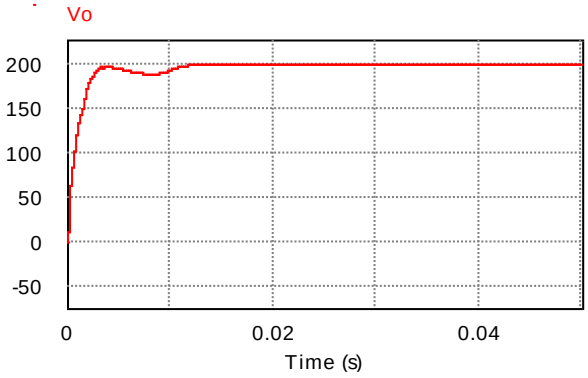


Fig. 9. Sweep baud diagram.

In order to make the converter have better stability and dynamic characteristics, the PI controller is used for control. Import the Bode diagram obtained by frequency sweep into the PID Tuner toolbox in Matlab/Simulink, adjust the PI parameters, and after compensation, the system step response curve can be seen from Figure 10 (a). Concurrently, in Figure 10. (b), joint simulation yields the simulation curve of the converter's output voltage. Comparing the step response in the toolbox with the electric curve in the joint simulation, it can be seen that the two curves are stable at about 0.015s after vibration, and the overall trend is consistent, which proves the correctness of the control system design.



(a) PID Tuner regulation system step curve



(b) Radio wave shape on joint simulation converter

Fig. 10. Comparison of simulation results.

4.3. Experimental Verification

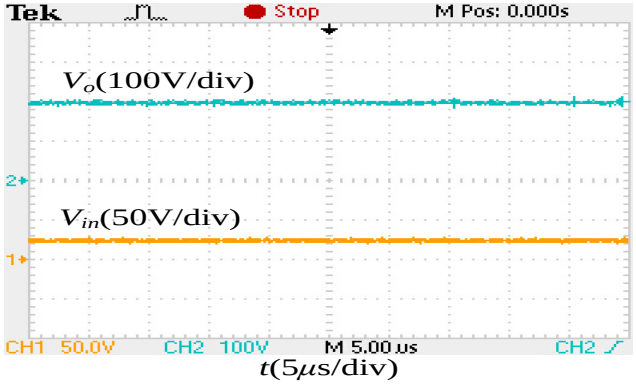
To confirm the accuracy of the coupled inductor Cuk-Sepic converter principle proposed in this paper, it created a testing prototype with an input voltage of 24V and a rated power of 150W. The control method of the prototype is a single voltage closed loop and its parameters are detailed in Table 2.

Table 2. Converter parameters

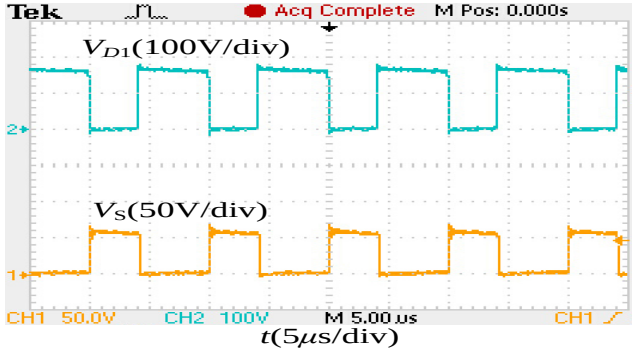
Parameter	Parameter Value
Input Inductance Li/μH	47
Oupling Inductance Turn Ratio n	Ns/Np
Leakage inductance Lk/μH	1.7
Inductance Lo/μH	100
Capacitance C1、C2、C3、C4、Co	C1: 100μF/100V; C2:47μF/100V; C3:47μF/100V; C4:22μF/250V; Co:100μF/250V
Switch tube S	IRF260N
Diode D1、D2、D3	D1:MBR20100CT; D2、D3: MBR20200CT
Switching Frequency f/kHz	100

Figure 11 displays the primary voltage waveform of the converter. By examining Figures 7(a) to (c), it is evident that the proposed converter yields an output voltage of 200V while keeping the voltage stress at a mere 60V. This value is much lower than the 200V output, resulting in lower voltage stress. Furthermore, the voltage stress of each diode is obvious lower compared to output voltage. These testing data verified the theoretical analysis precision.

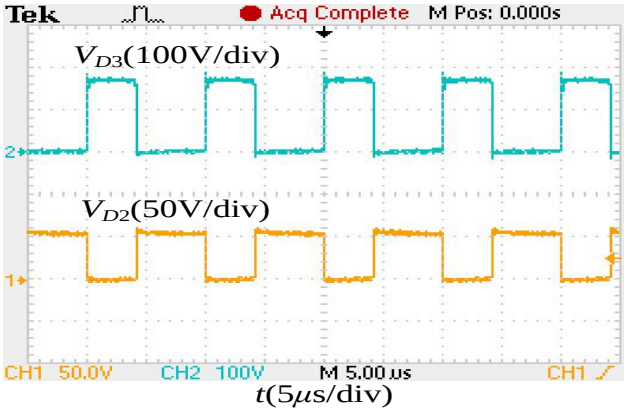
Figure 12 shows the main current waveform. According to this figure, the zero-current turn-off of diode D2 is achieved and diodes and realize zero-current turn-on. The input and output terminals possess inductance, allowing for a smooth flow of input and output current with minimal current ripple.



(a) Input and output voltage waveform

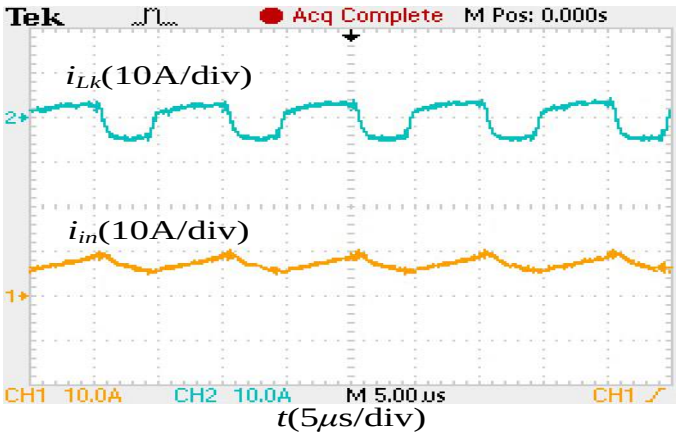


(b) Voltage waveform of switch tube S and diode D1

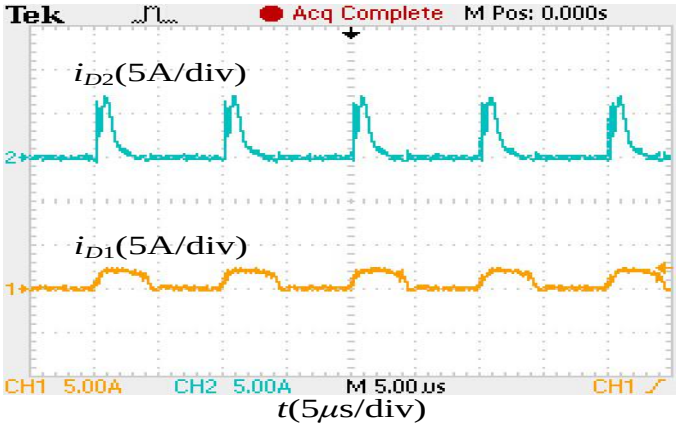


(c) Voltage waveform of diode D2 and D3

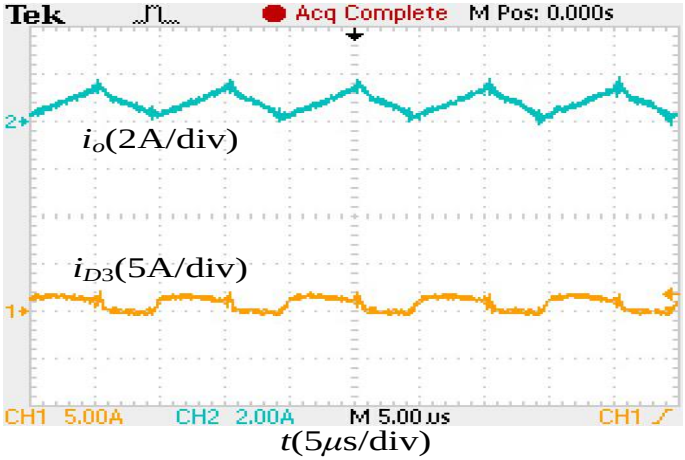
Fig. 11. Main voltage waveform of converter.



(a) Input inductor Li and primary current waveform of coupling inductor



(b) Voltage waveform of diode D1 and D2



(c) Diode D3 and output inductor Lo current waveform

Fig. 12. Main current waveform of converter.

Fig. 13 gives the prototype tested efficiency at 200V output voltage with different power. As can be observed, the prototype's highest efficiency is around 94.6%, and at its 150W rated efficiency, it can reach 93.9%.

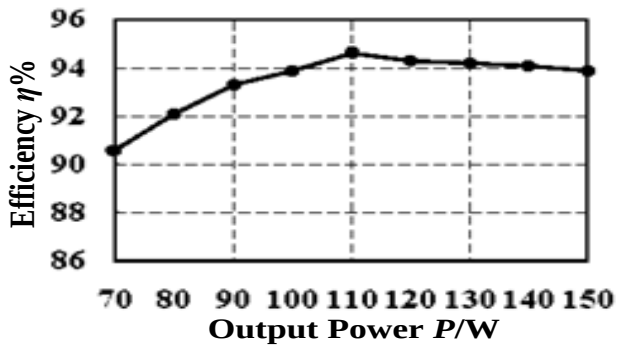


Fig. 13. Efficiency curve of prototype.

5. Conclusion

This study aims to design a high-gain Cuk-Sepic converter that integrates both the Cuk and Sepic converters and enhances the voltage-doubling structure of the coupling inductor to achieve better efficiency. Integrating both the Cuk and Sepic converters allows for improved performance and efficiency in voltage conversion. By combining the strengths of these two converter types, the designed high-gain Cuk-Sepic converter can achieve a better voltage-doubling structure and higher efficiency, resulting in reduced energy consumption and lower power losses. This integration also enables a compact design and reduced size, making it more suitable for various applications. The voltage gain of the coupling inductance was regulated based on the turn ratio n of coupling inductance to achieve a higher voltage gain. Integrating the Cuk and Sepic converters offers several advantages. By combining the strengths of these two converter types, the designed high-gain Cuk-Sepic converter can achieve better voltage conversion performance and efficiency. This reduces energy consumption and lower power losses, resulting in a more sustainable and environmentally friendly solution. Additionally, the integration allows for a compact design and reduced size, making the converter more suitable for various applications. Low voltage stress is also experienced by switching devices. Inductance is present at both ends of the converter, which reduces ripples in the converter's current.

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